



Description

JMT N-channel Enhancement Mode Power MOSFET

Features

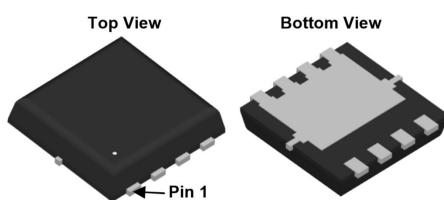
- 100V, 23A
- $R_{DS(ON)} < 32m\Omega$ @ $V_{GS} = 10V$
- $R_{DS(ON)} < 36m\Omega$ @ $V_{GS} = 4.5V$
- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

Application

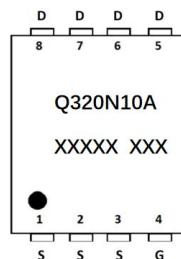
- Load Switch
- PWM Application
- Power management



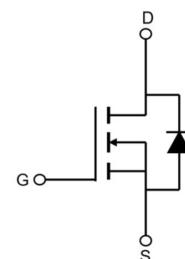
100% UIS TESTED!
100% ΔV_{ds} TESTED!



PDFN3x3-8L



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
Q320N10A	JMTQ320N10A	TAPING	PDFN3x3-8L	13inch	5000	50000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		100	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	23	A
		$T_C = 100^\circ C$	15	A
I_{DM}	Pulsed Drain Current ^{note1}		92	A
EAS	Single Pulsed Avalanche Energy ^{note2}		52.6	mJ
P_D	Power Dissipation	$T_C = 25^\circ C$	29	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		4.3	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ C$



JMTQ320N10A

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristics						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=100\text{V}$, $V_{GS}=0\text{V}$,	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.0	1.5	2.5	V
$R_{DS(\text{on})}$ note2	Static Drain-Source on-Resistance	$V_{GS}=10\text{V}$, $I_D=20\text{A}$	-	24	32	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=10\text{A}$	-	26	36	$\text{m}\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	3217	-	pF
C_{oss}	Output Capacitance		-	126	-	pF
C_{rss}	Reverse Transfer Capacitance		-	113	-	pF
Q_g	Total Gate Charge	$V_{DS}=30\text{V}$, $I_D=15\text{A}$, $V_{GS}=10\text{V}$	-	23	-	nC
Q_{gs}	Gate-Source Charge		-	5	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	4	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=30\text{V}$, $I_D=15\text{A}$, $R_G=1.8\Omega$, $V_{GS}=10\text{V}$	-	12.6	-	ns
t_r	Turn-on Rise Time		-	6	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	22	-	ns
t_f	Turn-off Fall Time		-	5.3	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	23	-	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	92	-	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}$, $I_S=23\text{A}$	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	$IF=23\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$	-	71	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	145	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition : $T_J=25^\circ\text{C}$, $V_{DD}=50\text{V}$, $V_G=10\text{V}$, $L=0.5\text{mH}$, $R_g=25\Omega$, $I_{AS}=14.5\text{A}$

3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

Typical Performance Characteristics

Figure 1: Output Characteristics

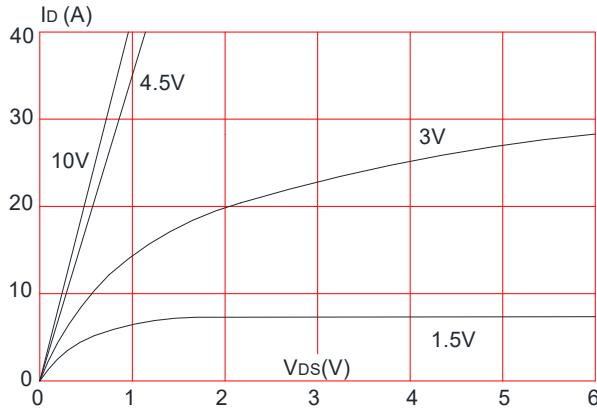


Figure 3: On-resistance vs. Drain Current

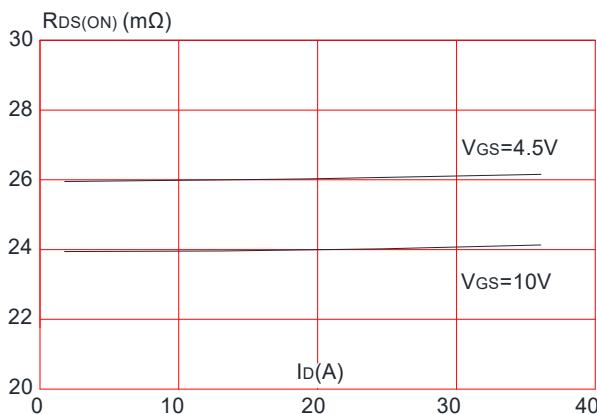


Figure 5: Gate Charge Characteristics

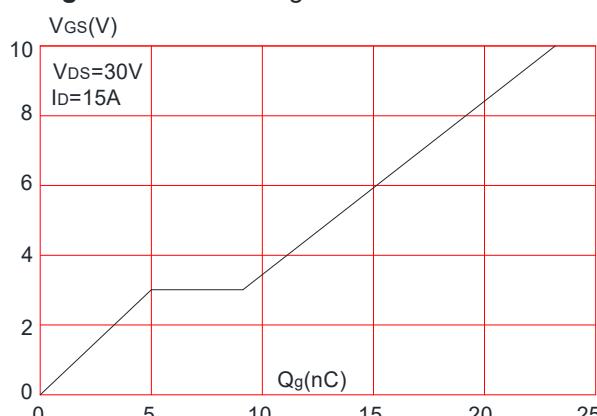


Figure 2: Typical Transfer Characteristics

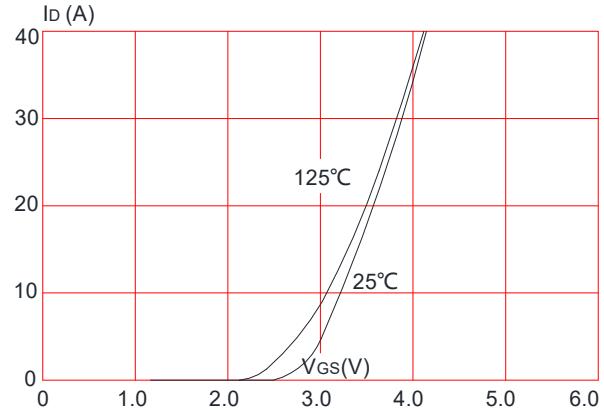


Figure 4: Body Diode Characteristics

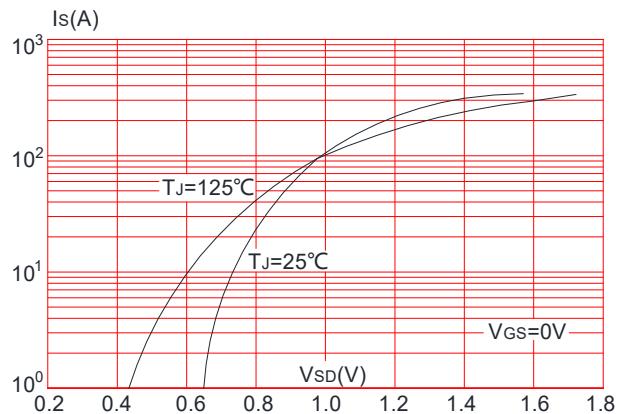


Figure 6: Capacitance Characteristics

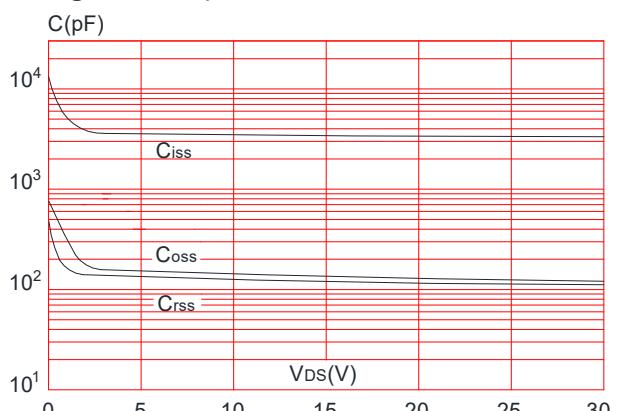


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

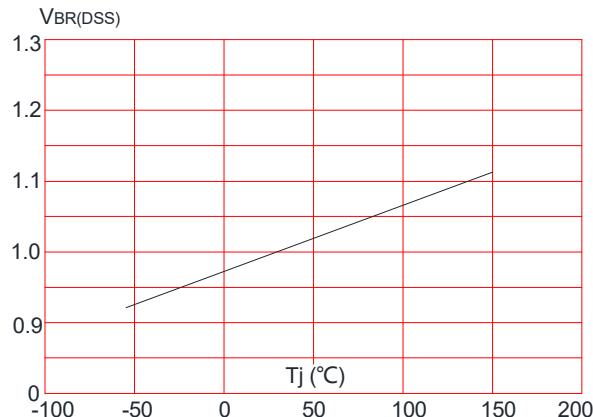


Figure 8: Normalized on Resistance vs. Junction Temperature

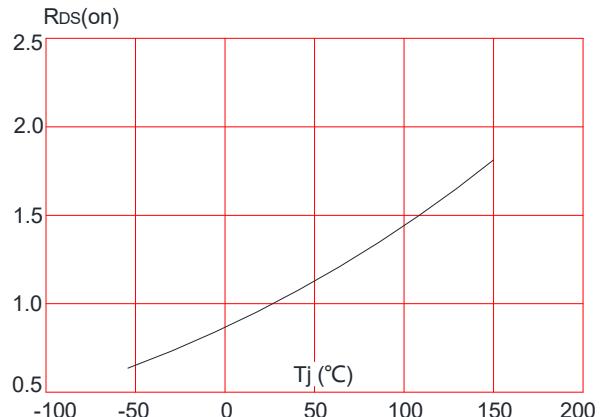


Figure 9: Maximum Safe Operating Area

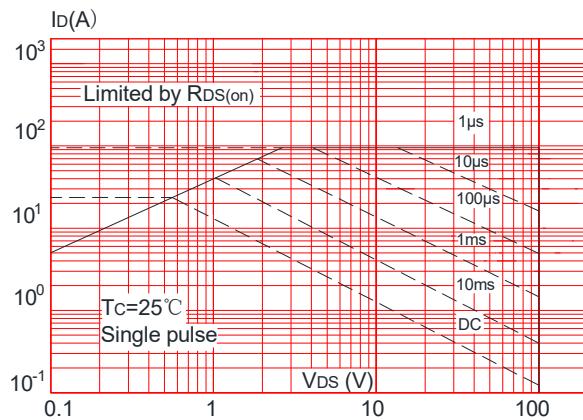


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

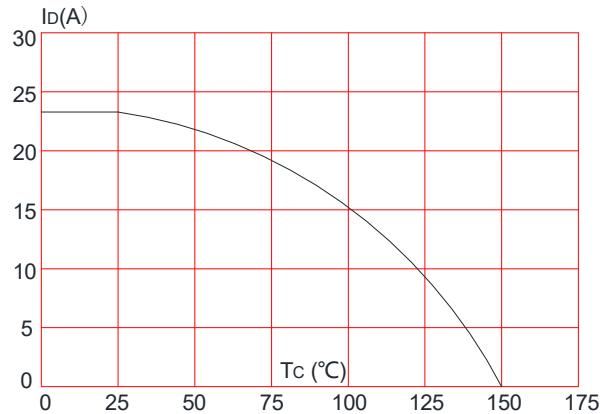
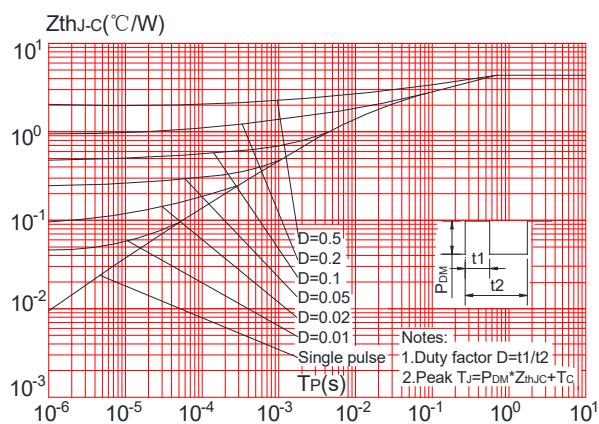


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test Circuit

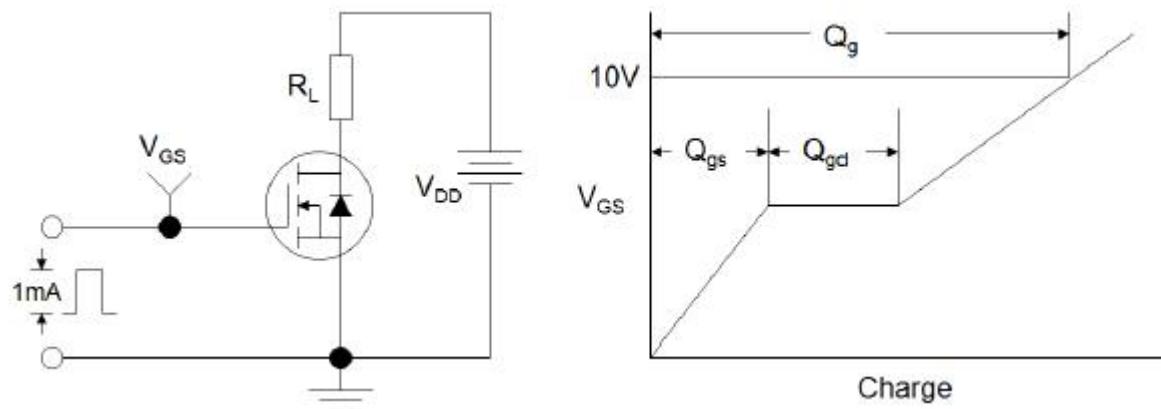


Figure1:Gate Charge Test Circuit & Waveform



Figure 2: Resistive Switching Test Circuit & Waveforms

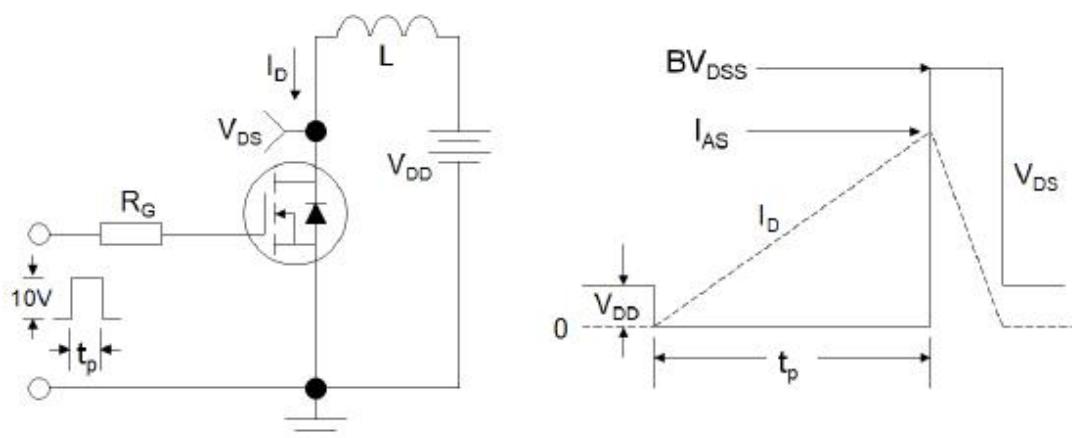
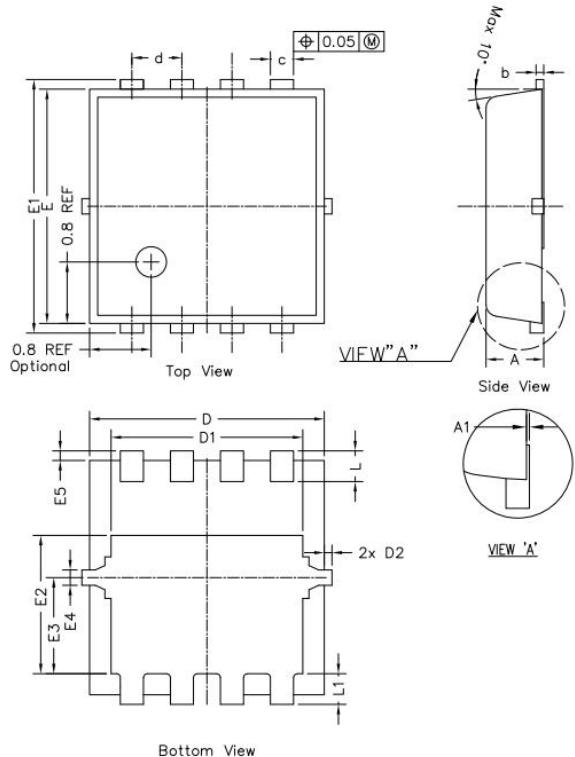


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



Package Mechanical Data- PDFN3x3-8L



SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	---	---	0.050	----	----	0.002
b	0.144	0.152	0.202	0.006	0.006	0.008
c	0.250	0.300	0.350	0.010	0.012	0.014
d	0.65 BSC			0.026 BSC		
D	2.950	3.050	3.150	0.116	0.120	0.124
D1	2.390	2.490	2.590	0.094	0.098	0.102
D2	---	---	0.125	---	---	0.005
E	2.950	3.050	3.150	0.116	0.120	0.124
E1	3.200	3.300	3.400	0.126	0.130	0.134
E2	1.700	1.800	1.900	0.067	0.071	0.075
E3	1.150	1.250	1.350	0.045	0.049	0.053
E4	0.150	0.200	0.250	0.006	0.008	0.010
E5	0.075	0.125	0.175	0.003	0.005	0.007
L	0.300	0.400	0.500	0.01	0.02	0.02
L1	0.300	0.400	0.500	0.01	0.02	0.02

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